

WHAT IS CLAIMED IS:

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- 1 1. A processor comprising:
- 2 means for executing an instruction of an application of a first bit size ported to a
- 3 second bit size environment, the second bit size being greater than the first bit size; and
- 4 means for confining the application to a first bit size address space subset.
- 1 2. The processor of claim 1, wherein the first bit size is 32-bit and the second bit
- 2 size is 64-bit.
- 1 3. The processor of claim 1, wherein the means for confining includes:
- 2 means for truncating generated address references of the second bit size to the first
- 3 bit size; and
- 4 means for extending to the second bit size the truncated generated address
- 5 references.
- 1 4. The processor of claim 3, wherein the means for confining includes means for
- 2 generating an address fault.
- 1 5. The processor of claim 1, wherein the means for extending includes means for
- 2 determining that the first bit size address space subset is signed address space.
- 1 6. The processor of claim 1, wherein the means for extending includes means for
- 2 determining that the first bit size address space subset is unsigned address space.

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1 7. A processor comprising:
2 a memory to store an instruction of an application ported from a first bit size
3 environment to a second bit size environment, the second bit size being greater than the
4 first bit size; and
5 an instruction execution core coupled to said memory, said instruction execution
6 core to execute the instruction of the application, said instruction execution core to
7 determine that the application is confined a first bit size address subset;
8 generate an address reference of the second bit size as part of execution of the
9 instruction;
10 truncate the generated address reference from the second bit size to the first bit
11 size; and
12 extend the truncated, generated address reference from the first bit size to the
13 second bit size.

1 8. The processor of claim 7, wherein the application ported from a first bit size
2 environment to a second bit size environment is an application ported from a 32-bit
3 environment to a 64-bit environment.

1 9. The processor of claim 7, wherein the instruction execution core is to determine
2 that the application is confined to a first bit size address subset based at least in part on
3 an address space control flag.

1 10. The processor of claim 7, wherein the instruction execution core is to extend the
2 truncated, generated address reference from the first bit size to the second bit size based
3 at least in part on an address format control flag.

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1 11. The processor of claim 7, wherein the instruction execution core is to generate
2 an address fault flag based least in part on a comparison of the generated address
3 reference and the extended, truncated, generated address reference.

1 12. The processor of claim 11, wherein the instruction execution core is to generate
2 an address fault flag based least in part on an address fault control flag.

1 13. The processor of claim 7, wherein said memory is a cache memory.

1 14. The processor of claim 7, wherein the processor is a 64-bit processor.

1 15. A method to confine an application to an address space subset, the method
2 comprising:

3 determining that an application is confined a first bit size address subset, the
4 application including an instruction;

5 generating an address reference of the second bit size as part of execution of the
6 instruction;

7 truncating the generated address reference from the second bit size to the first bit
8 size; and

9 extending the truncated, generated address reference from the first bit size to the
10 second bit size.

1 16. The method of claim 15, wherein the application is ported from a first bit size
2 environment to a second bit size environment.

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1 17. The method of claim 16, wherein the application ported from a first bit size
2 environment to a second bit size environment is an application ported from a 32-bit
3 environment to a 64-bit environment.

1 18. The method of claim 15, wherein determining that an application is confined a
2 first bit size address subset, the application including an instruction is based at least in
3 part on a address space control flag.

1 19. The method of claim 15, wherein extending the truncated, generated address
2 reference from the first bit size to the second bit size is based at least in part on an
3 address format control flag.

1 20. The method of claim 15, wherein extending the truncated, generated address
2 reference from the first bit size to the second bit size includes sign-extending the
3 truncated, generated address reference from the first bit size to the second bit size based
4 at least in part on an address format control flag.

1 21. The method of claim 15, wherein extending the truncated, generated address
2 reference from the first bit size to the second bit size includes zero-extending the
3 truncated, generated address reference from the first bit size to the second bit size based
4 at least in part on an address format control flag.

1 22. The method of claim 15, wherein extending the truncated, generated address
2 reference from the first bit size to the second bit size includes generating an address
3 fault flag based least in part on a comparison of the generated address reference and the
4 extended, truncated, generated address reference.

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23. The method of claim 22, wherein generating an address fault flag is based least

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in part on an address fault control flag.